Al-Mansoura University
Faculty of Engineering
Communications and Elect. Dept

Logic Circuits 2
2nd Year Students
Time 3 Hours

Attempt in all questions and assume any missing data.

Q1-Draw the following logic circuits, explain its operations, and write its truth table:

1- Active-low S-R latch
2- Gated S-R latch.
3- Positive edge triggered D flip flop.
4- Negative edge triggered J-K flip flop with asynchronous reset and clear inputs.

Q2:-(a):-Design a frequency divider circuit using a J-K positive edge triggered flip flop. Input waveform has a frequency 16 k Hz, and the output waveform has a frequency 1 k Hz.

(b):-For a negative edge-triggered J-K flip-flop with the inputs shown in Figure 1, develop the Q output waveform relative to the clock. Assume that Q is initially LOW.

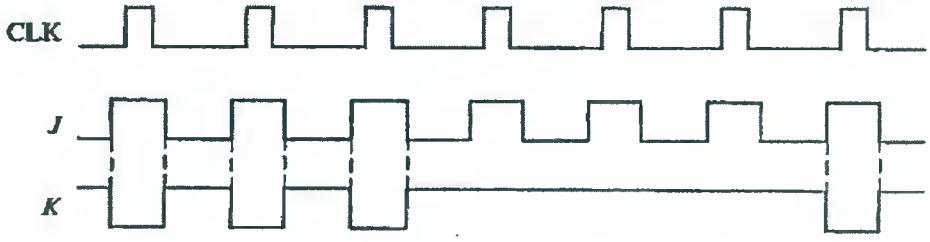

Figure (1)

Q3-Design the following counters:

1- A 3-bit asynchronous binary counter with timing diagram.
2- A 4-bit synchronous counter with timing diagram.
3- A synchronous BCD counter.
4- A 3-bit up/down synchronous binary counter.

Q4- Implement the decoding of binary state 2 and binary state 7 of a 3-bit synchronous counter. Show the entire counter timing diagram and the output waveforms of the decoding gates.

Q5-Design the following shift registers:

1- Serial in/Parallel out.
2- Parallel in/Serial out.
3- Bidirectional.
4- Serial in/Serial out.

Q6- Serial data transmission from one digital system to another is commonly used to reduce the number of wires in the transmission line. Design a serial-to-parallel data converter to solve this problem for the serial data format shown in Figure (3).

Figure (3)

Q7- (a): Draw the block diagram of a 3-dimensional RAM memory showing address bus, address decoders, bidirectional data bus, and read/write inputs. Explain the function of each component.

(b): Explain with drawing the following basic operation of the DRAM:
(1)-Writing a 1 into the memory cell.
(2)-Writing a 0 to memory cell.
(3)-Reading a 1 from the memory cell.
(4)-Refreshing a stored 1.